Amendments to the Claims:

The below listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (currently amended) A CAM (content addressable memory) apparatus ~~having~~ comprising:

a first memory device ~~(10)~~ with a word line input ~~(WL)~~ and at least one storage node ~~(12; 13)~~ for storing a first bit of a data word;

a second memory device ~~(11)~~ with a word line input ~~(WL)~~ and at least one storage node ~~(14; 15)~~ for storing a second bit of a data word; and

a comparator device ~~(16)~~ for comparing the first and second stored bits with ~~two~~ first and second precoded comparison bits fed via four inputs ~~(20; 21; 22; 23)~~ and for driving a hit node ~~(17)~~ in the event of the first stored bit corresponding to the first comparison bit and the second stored bit corresponding to the second comparison bit.

2. (currently amended) The CAM apparatus according to Claim 1, ~~characterized in that~~ wherein the comparator device ~~(16)~~ has four signal paths ~~via in~~ each having ~~case~~ three transistors ~~(P; N)~~ between a supply voltage ~~(V_v)~~ and the hit node ~~(17)~~.

3. (currently amended) The CAM apparatus according to Claim 2, ~~characterized in that~~ wherein the comparator device ~~(16)~~ has a series-parallel circuit comprising twelve field-effect transistors ~~(P; N)~~ of a first conduction type.

4. (currently amended) The CAM apparatus according to Claim 3, ~~characterized in that~~ wherein the comparator device ~~(16)~~ has four parallel-connected series circuits comprising in each case three field-effect transistors ~~(P; N)~~ of the first conduction type.

5. (currently amended) The CAM apparatus according to Claim 2, ~~characterized in that~~ wherein the comparator device ~~(16)~~ has a series-parallel circuit comprising eight field-effect transistors ~~(P; N)~~ of a first conduction type.

6. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 2 ~~to 5~~, ~~characterized in that~~ wherein a first, second, third and fourth storage node ~~(12; 13; 14; 15)~~ of the memory devices ~~(10; 11)~~ are connected to gate terminals of a first and second field-effect transistor ~~(P; N)~~ of the first conduction type of a respective path of a series-parallel circuit in such a way that precisely one path can be switched through by each of the four bit combinations possible from two bits.

7. (currently amended) The CAM apparatus according to Claim 6, ~~characterized in that~~ wherein a respective third transistor of each one of the four paths is connected, on the gate side, ~~in each case~~ to a respective one of the four inputs ~~(20, 21, 22, 23)~~ for ~~feeding~~ inputting the ~~two~~ first and second precoded comparison bits.

8. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 3, ~~characterized in that~~ wherein the comparator device ~~(16)~~ has a field-effect transistor ~~(N; P)~~ of a second conduction type ~~with a control terminal (18),~~ which differs from the first conduction type, the field-effect transistor having a control terminal and ~~is~~ located between the hit node ~~(17)~~ and a reference potential ~~(V_M)~~.

9. (currently amended) The CAM apparatus according to Claim 8, ~~characterized in that~~ wherein the four input lines comprise four comparison lines and the field-effect transistor (N; P) of the second ~~power [sic]~~ conduction type can be switched through via the control terminal ~~(18)~~ if all of the comparison lines ~~(20, 21, 22, 23)~~ have a predetermined signal level.

10. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 3, ~~characterized in that~~ wherein the comparator

device ~~(16)~~ has four series-connected field-effect transistors ~~(N; P)~~ of a second conduction type, which differs from the first conduction type.

11. (currently amended) The CAM apparatus according to Claim 10, ~~characterized in that~~ wherein the four field-effect transistors ~~(N; P)~~ of the second conduction type are connected in series with a series-parallel circuit comprising field-effect transistors ~~(P; N)~~ of the first conduction type between the hit node ~~(17)~~ and a reference potential ~~(V_M)~~.

12. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 3 ~~to 11~~, ~~characterized in that~~ wherein the field-effect transistors ~~(P; N)~~ of the first conduction type form a p channel and the field-effect transistors ~~(N; P)~~ of the second conduction type form an n channel.

13. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 3 ~~to 11~~, ~~characterized in that~~ wherein the field-effect transistors ~~(P; N)~~ of the first conduction type form an n channel and the field-effect transistors ~~(N; P)~~ of the second conduction type form ~~an~~ a p channel.

14. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 1, ~~characterized in that~~ wherein the comparator device ~~(16)~~ has a holding device ~~(30)~~ for maintaining a signal level at the hit node ~~(17)~~.

15. (currently amended) The CAM apparatus according to Claim 14, ~~characterized in that~~ wherein the holding device has three transistors, of which a first transistor of the three transistors and a second transistor of the three transistors ~~form~~ forms an inverter ~~(I),~~ the input of which is connected to the hit node ~~(17),~~ and the output of which is connected to a gate of ~~the~~ a third transistor ~~(N; P)~~ of the three transistors.

16. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 1, ~~characterized in that~~ wherein a circuit ~~which~~ that is upstream of the CAM apparatus ~~and serves for generating~~ generates the two precoded comparison bits and can be operated statically or dynamically.

17. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 1, ~~characterized in that~~ wherein both a downstream series pass gate hit path and a wired-Or hit path can be driven via the hit node ~~(17)~~.

18. (currently amended) The CAM apparatus according to ~~one of the preceding Claims~~ Claim 1, ~~characterized in that~~ wherein the memory devices ~~(10; 11)~~ are in each case constructed identically and in each case have six transistors, four of which form two antiparallel inverters (I).